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Timing/Phase Reference Development for APS SPX

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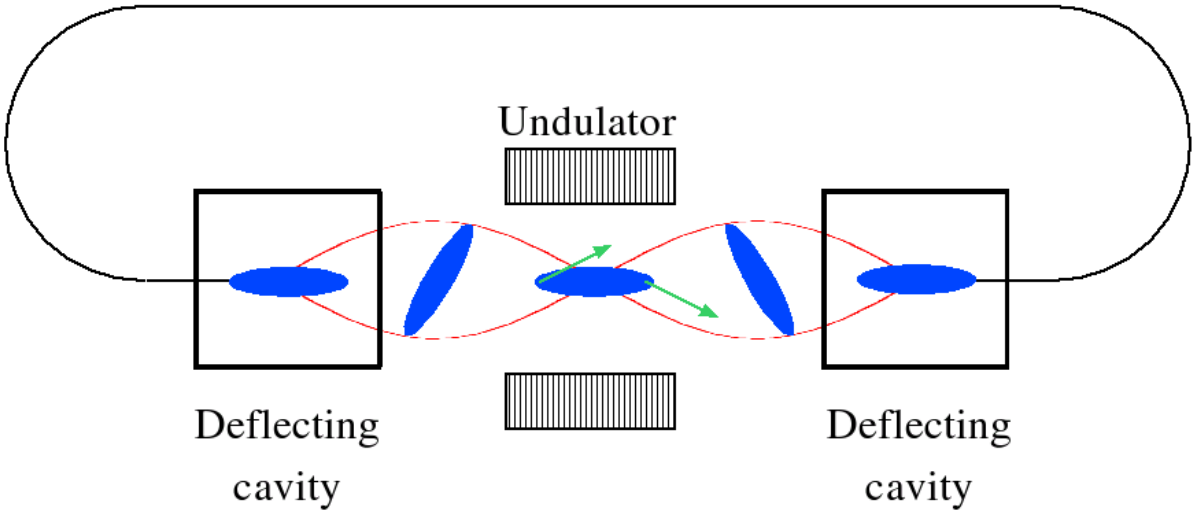
SPX Goals

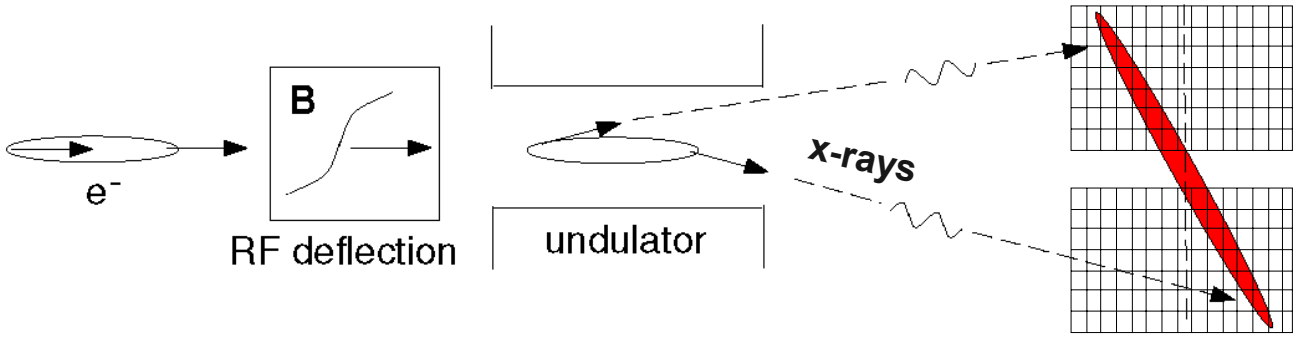
- ~ 1 ps pulses
- Energy tunability
- Flux comparable to 100 ps
- High repetition rate
- No impact on emittance
- Current Stability

Goals and Constraints

- X-ray pulse length below 4ps.
- Must have 1KHz rep. rate for source to be scientifically useful.
- Hybrid fill pattern only (chirp applied to 16mA bunch).
- Phase I - provide initial capability
  - – ‘Few’ picoseconds x-ray pulse length, 120Hz rep rate.
- Phase II
  - – (a) Increase rep. rate to 1KHz (new klystron and modulator)
  - – (b) Reduce x-ray pulse length to ~1ps (long ID straight)

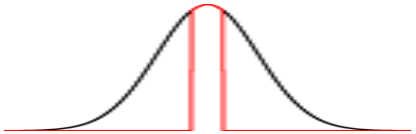
Short-pulse generation with rf deflection†





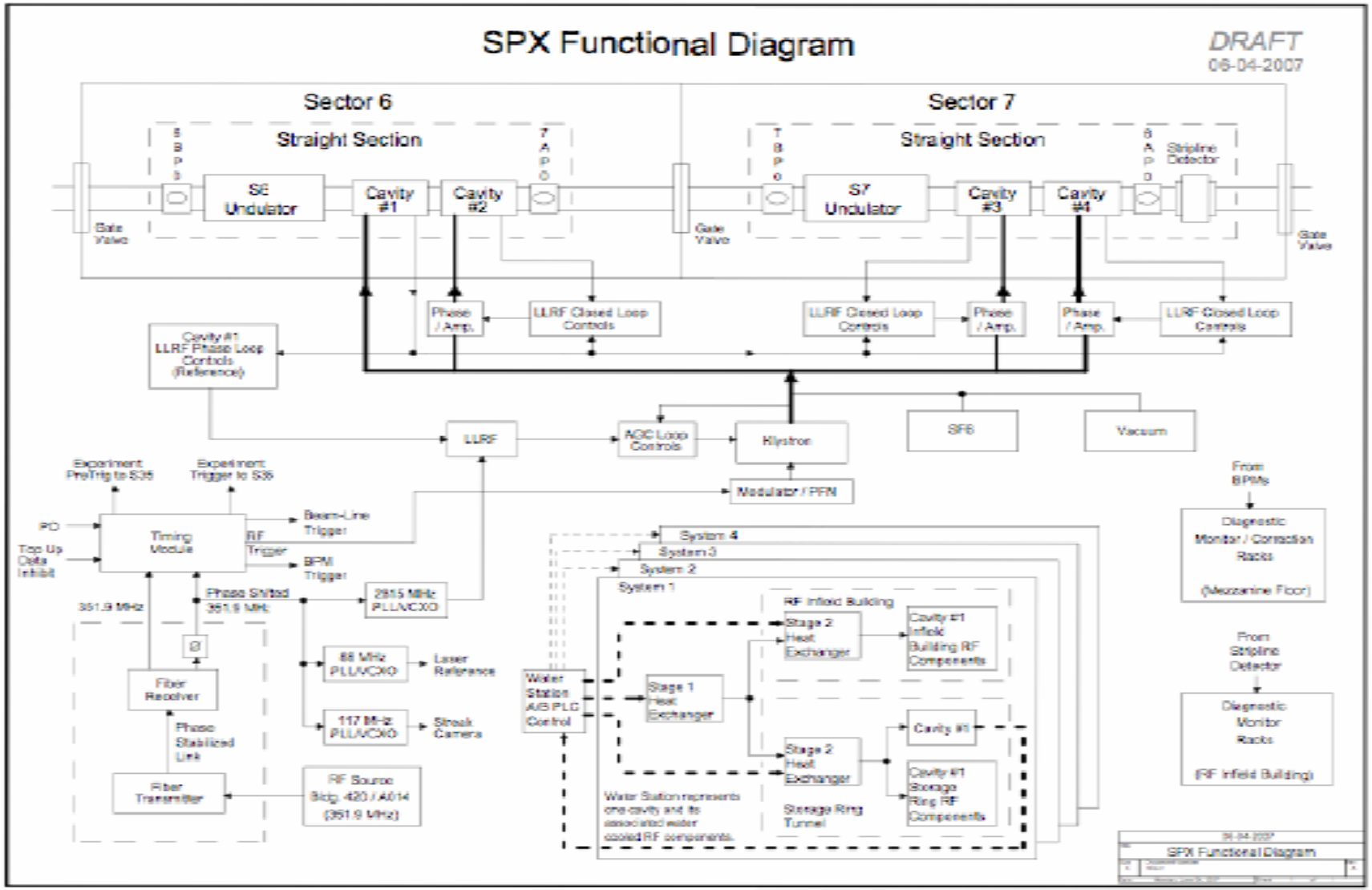
Slits can be used to clip out a short pulse.

Can also use asymmetric cut crystal to compress the pulse.



† A. Zholents, P. Heimann, M. Zolotorev, J. Byrd, NIM A 425 (1999)

SPX Functional Diagram



Project Schedule

- 4/2008 Install 2 unpowered cavities in S7
- 9/2008 Install remaining systems and begin comissioning

Tolerances

- Table 1: Tolerances for Crab Cavities Assuming 4 MV Limit for Long-Straight Case

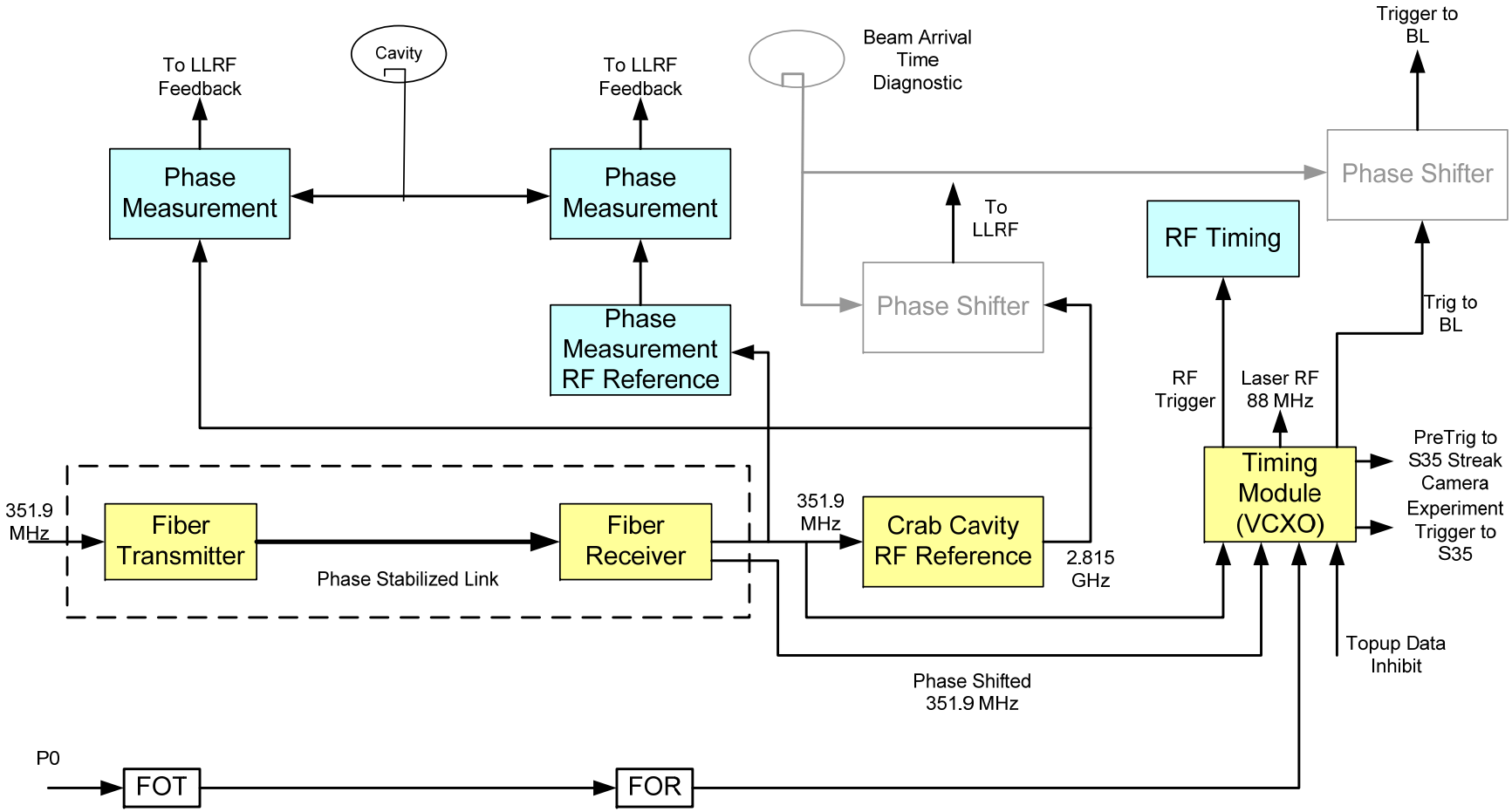
Case	Phase Deg	Voltage %
Static/Slow LS 1 kHz (Uncorrelated)	0.075	0.15
Static/Slow SS 120 Hz (Uncorrelated)	0.22	0.39
Pulse-to-Pulse	0.8	1

Ref: Tolerances for Pulsed Crab Cavities in a Single Straight Section
OAG-TN-2006-051
Michael Borland—10/16/2006

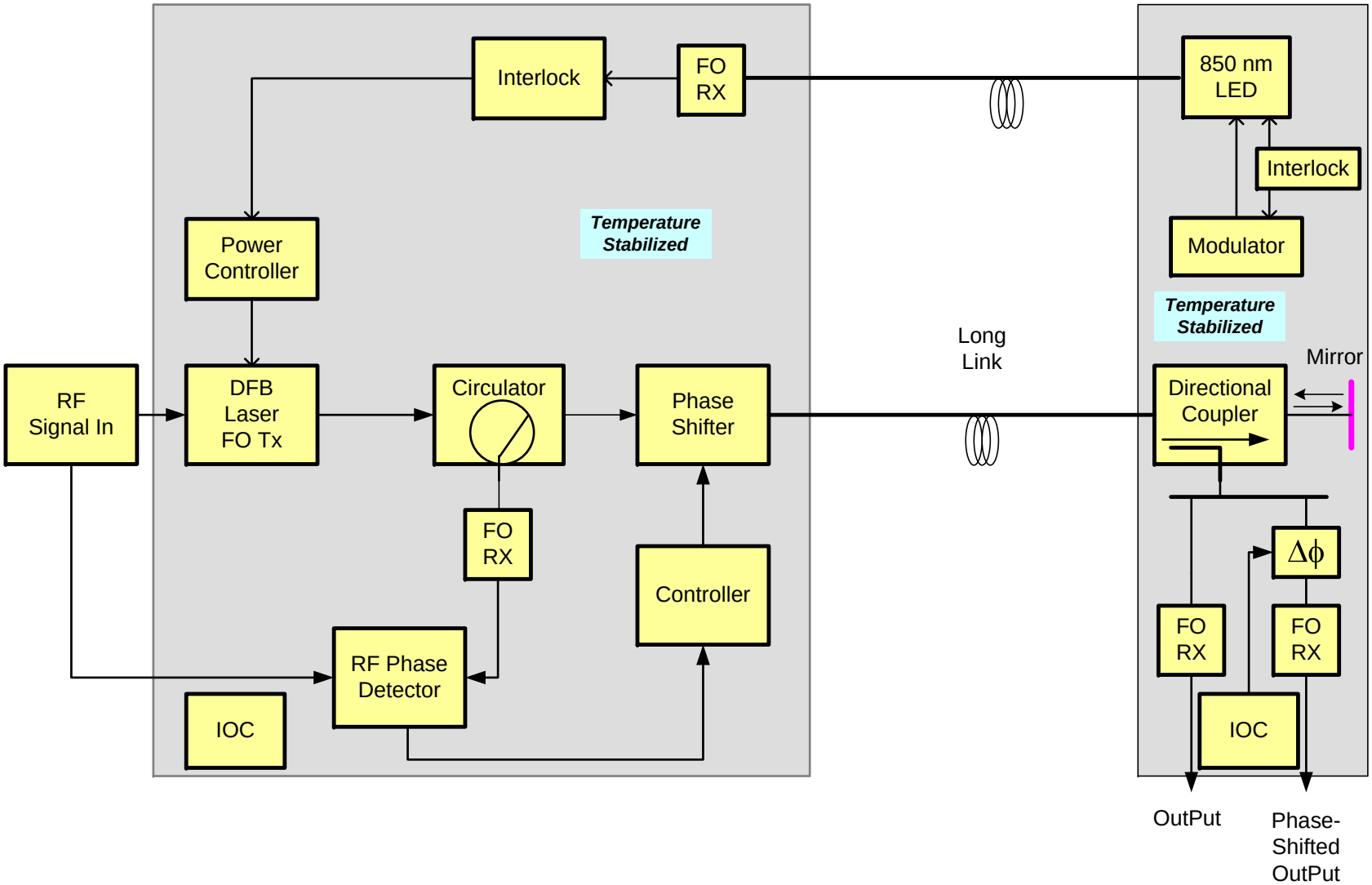
Note:

From ILC RDR: Stability at the point of RF measurement and control has to be ~10 picoseconds. The more demanding bunch compressors require a short-term stability of ~100 femtoseconds

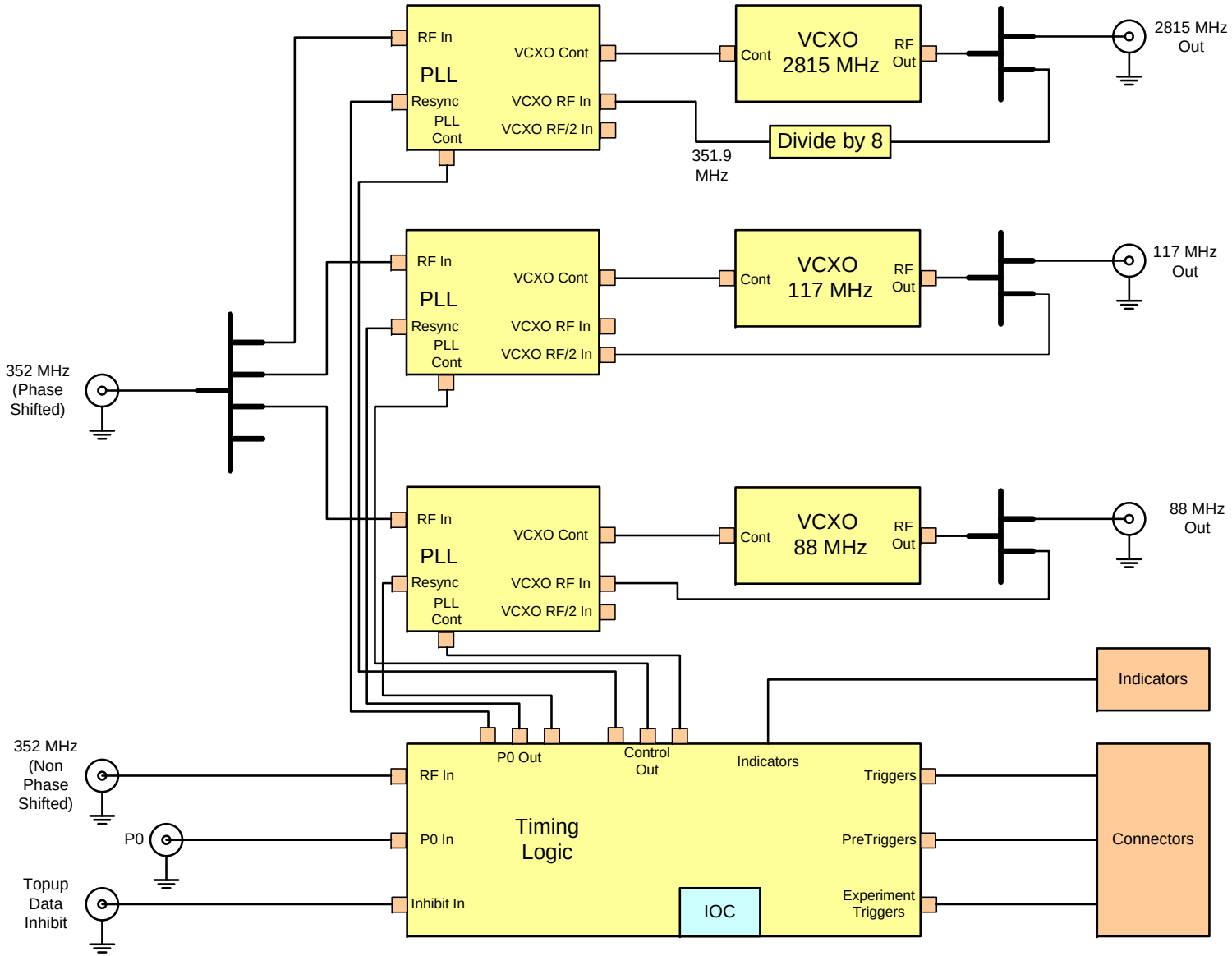
Timing/Phase Reference



Phase Stabilized Link with Interlock



Timing/RF references



Initial Results

- 2815 MHz PLL testing
- Computed 2815 MHz VCXO RMS Jitter from Vendor supplied data
  - ~90 femtoseconds (10 Hz to 270 kHz) (0.09 degrees @ 2815 MHz)
- Crude Measurement
  - 770 femtoseconds (0.5 Hz to 4 GHz) Agilent 54854A DSO, 4 GHz, 20 GSa/s (Corrected for reference and DSO jitter)
- Computed
  - 595 Femtoseconds (10 Hz to 4 GHz)

Status

- Most components ordered and received
  - All VCXOs
  - Most Optical Components
- Revised PLL board in fabrication
- Prototype Timing Board in Test
- Fiber Link in detailed design