

10.3 BCD Proposal: Diagnostic Interlock Layer (DIL)

1. Overview

The Diagnostic Interlock Layer is a proposed new control layer for High Availability (HA) design of the power systems in the ILC. Hard interlocks between power sources such as magnet power supplies and klystron modulators are typically a major cause of machine interruption. Typically interlocks for systems are summed into chains and often lack diagnostics to quickly isolate faults and return the machine to service. A new Diagnostic Interlock Layer (DIL) is envisaged to solve this problem in the ILC. All modules in a power system would be equipped with such a diagnostic with the capabilities of checking the health of the systems board-by-board and displaying summaries at any time in the control room. The DIL could have the local intelligence to take actions to avoid impending trips due to over-voltage, over-current or over-temperature. It also could read out critical switching waveforms for example to pinpoint problems before they cause a shutdown. Evasive actions could include lowering current or voltage in a module while others compensate, turning off a faulty unit and flagging maintenance to hot swap it before another failure interrupts the machine. Special network hardware, software, controls and displays are envisaged that are accessible to operators and maintenance technicians from any location in the accelerator complex.

2. DIL Design Principles

The DIL main component is a small embedded card or chip that drops into a variety of power components. The idea is modeled after the commercial Intelligent Platform Management (IPM) system of the Telecom modular standard known as ATCA. In ATCA IPM performs the following tasks:

1. Senses faults in an individual carrier module or mezzanine module (subunit).
2. Removes primary power from the module (while retaining control power at all times)
3. Reports to main control that a module has failed, and lights a front panel LED to indicate it is safe to hot-swap.
4. After hot-swap, recognizes the new module type and power requirements.
5. Authorizes the delivery of primary power after checking that the Shelf total power will not be exceeded.
6. Monitors temperatures and power consumption of all modules in the Shelf.
7. Monitors for fan failures, and when one occurs, rearranges speed of the other fans (four total) to compensate, while reporting to main control the need to hot-swap one of the fans.
8. Other features can be programmed into the Shelf level at user discretion.

3. DIL Implementation in the ILC

In the ILC the DIL will be part of a site-wide IPM system. Typically it would remotely set and monitor interlock trip limits, measure and display timing and trigger functions, and

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capture important waveforms. A response to impending or actual trips may be taken locally or by a higher controls layer. Operations and maintenance will routinely monitor the diagnostic layer to observe the health of running systems or to trace anomalous behavior. The following are some example DIL implementations:

1. Modulator

Each *module* of a modulator contains a DIL sub-unit, such as an ATCA mezzanine board, which provides information constantly to the imbedded DIL *unit* manager, and secondarily to the *master system* at main control. See Fig. 1. Typical features are:

- Disable a faulty module and restore total voltage output without machine turnoff..
- Raise fan speed to compensate for increased module temperature.
- Signal for replacement of failed modules or fans.
- Send all diagnostic information to main control.
- Capture important waveforms in memory on fault.

Quick repair of failed modules guarantees near 100% *system availability* and minimizes the number of *spare units* needed in the total modulator subsystem.

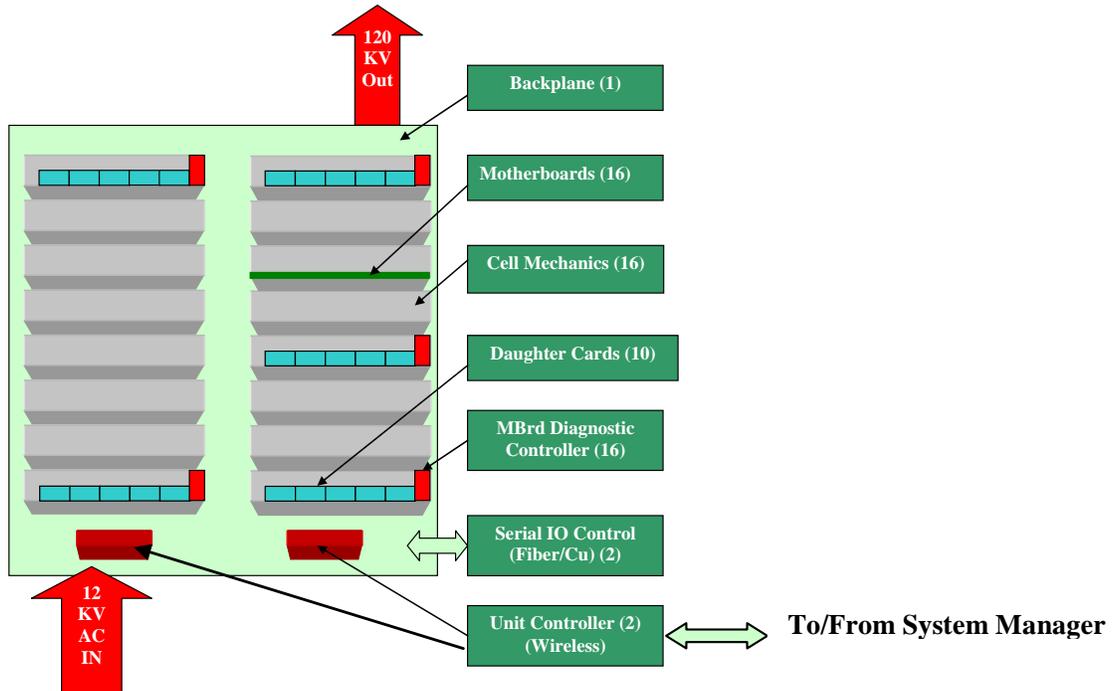


Fig.1. Modulator Diagnostics Interlock Layer

2. DC Power Supplies

DC power supplies designed as 1/n modular units gain similar advantages using a DIL as in the modulator example. The concept is shown in Fig. 2. A smaller multichannel supply can include a switchable spare channel as shown in Fig. 3. All units will contain DIL diagnostics chips or small boards.

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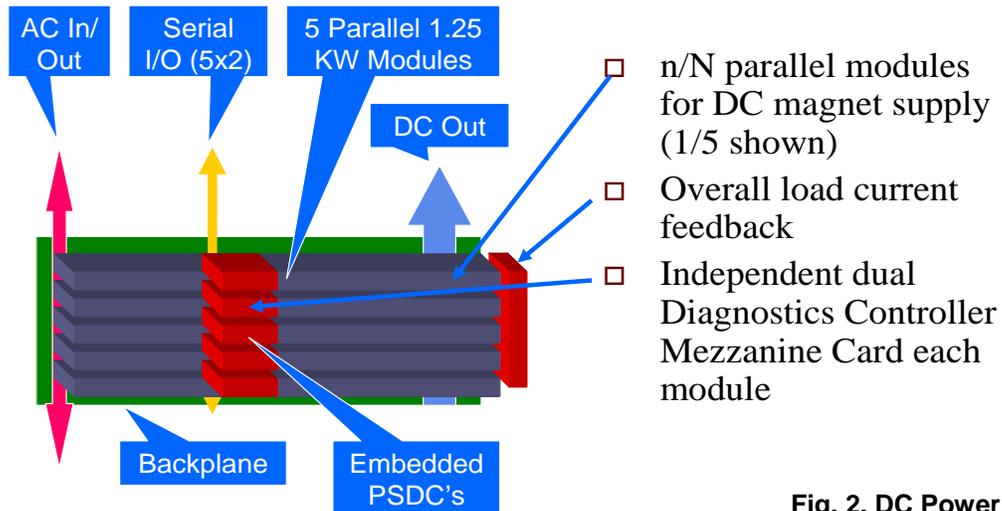


Fig. 2. DC Power Supply Diagnostics Interlock Layer

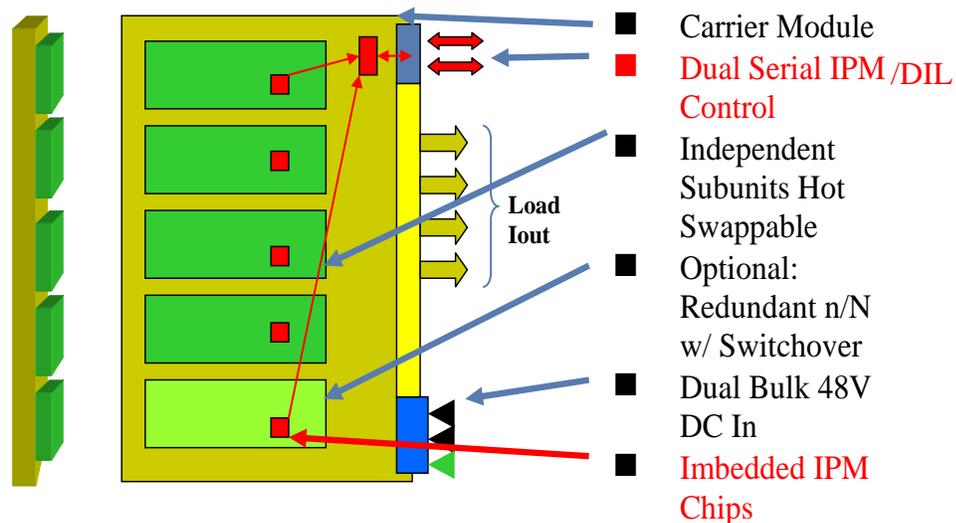


Fig.3. Corrector Subunit Supplies on Carrier Module with Imbedded IPM/DIL System

3. Instrument Modules

The DIL layer in instrument modules will primarily be the ATCA IPM layer. All the hooks for basic platform management and hot swap will be part of a standard commercial chip. All higher level trip-avoidance strategies will be programmed at the central computer IOC level.

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4. Interlock Trip-Avoidance

The system will be designed to *avoid* various kinds of trips by appropriate strategies.

Examples are:

- Track temperature of power components and reduce power or raise trips with local intelligence.
- Magnet over-temperature monitoring by analog means, such as resistance monitoring, in addition to klixon protection to detect, report normally hidden faults.
- Integrate flow switches to eliminate nuisance trips due to bubbles; monitor temperature of device as final protection trip source; schedule backflush, inspection on routine basis by remote valve control.
- Shut off LLRF level and Modulator source immediately on klystron or waveguide arc and compensate with standby station by MPS timing action.
- Process RF stations under independent algorithm control at each station to minimize processing time as well as arcing.
- Develop quick diagnostic and recovery strategies for tuners that lose reference during operation; work around failed or stuck tuners; compensate for loss of beam power automatically for mistuned but still functioning station.
- Detect and report tripped off pumps, cable faults. Systems are redundant so loss of one pump is tolerable. Repair while machine operates except for cable end in machine tunnel.

It's unclear how to apply DIL to cryogenics instrumentation, which consists primarily of temperature and pressure monitoring along the machine, with constant feedback to the main cryogenic plants. Ideally, but not likely, cryogenic systems should have 1/n redundancy to work around a failed or compromised unit. Modular system design should be investigated.

5. DIL Initiative: Power System Control Board (PSCB)

A DIL board with generic features for power systems monitoring is under development, to be used first on the Marx modulator. Provides independent trigger timing and pulse width control for each stage; fiber-optic isolation; IGBT temperature monitoring; transient waveform capture, monitor and set voltage references etc. See Ref. 1.

6. References

1. Diagnostic Interlock Layer, Draft, Ray Larsen.

<http://docdb.fnal.gov/ILC/DocDB/0001/000103/001/10.3.R.1%20DIL%20Draft%20110105.doc>

2. Performance Specification for the Power System Control Board (PSCB), PS-390-000-01, Rev. August 15 2005, P. Bellomo et al.

<http://docdb.fnal.gov/ILC/DocDB/0001/000102/001/10.3.R.2%20PSCB%20Performance%20Specification%20R1.doc>

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7. Cost Estimation

The DIL system consists of standard commercially available components, printed circuit assemblies, fiber networks and system controllers. A bottom-up system cost estimate will be made following GDE standard cost procedures.

8. R&D Path

- Complete prototype hardware, software, interface to control system (FY06)
- Test on Marx prototype modulator (FY07)
- Develop HA software layer to test integrated features on HA platform (FY07)
- Develop, test highly integrated version of DIL hardware (FY07-8)

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